The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte TSUYOSHI HIGUCHI and YOSHINORI OKAJIMA

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Appeal No. 1999-1131
Application No. 08/754,758

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HEARD: July 12, 2001

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Before JERRY SMITH, FLEMING, and GROSS, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-18, all the pending claims.

The instant invention relates to a pin arrangement of semiconductor devices and a pin arrangement of systems using semiconductor devices. Appellants' Specification

("Specification"), page 1, lines 6-10. Specification, page 5, line 35 to page 6, line 3. The principle of the invention aims to provide signal lines (control-signal lines and data-signal lines), other than power-signal lines, in a simple wiring layout using a small number of wiring layers. Specification, page 8, lines 5-9. Specifically, the semiconductor device arrangement includes control signal pins arranged on a first side, data-input/output pins arranged on a second side substantially perpendicular to the first side, and power-input pins provided on arbitrary sides of the semiconductor device. Specification, page 5, line 35 to page 6, line 3. In this manner, the pin arrangement according to the principle of the present invention can provide connections between semiconductor devices by using a small number of wiring layers and a simple wiring layout. Specification, page 8, lines 12-16. Since there is no branch stemming from the control-signal lines, signal reflections can be avoided to achieve high speed data transmission using high-frequency signals. Specification, page 8, lines 16-19.

Appellants' independent claims encapsulate the various embodiments of the invention. Independent appealed claims 1, 10, 14 and 18 are herein respectively recited:

1. A semiconductor device connected to one or more semiconductor devices of the same type, said semiconductor device comprising:

first pins for receiving signals commonly used with said one or more semiconductor devices; and

second pins for being connected to signal lines which are not connected to said one or more semiconductor devices,

wherein all of said first pins are provided on a first side of said semiconductor device and all of said second pins are provided on a second side of said semiconductor device substantially perpendicular to said first side, said first pins and said second pins excluding pins for receiving power voltages.

10. A semiconductor device comprising:

a semiconductor chip;

a package housing said semiconductor chip;

first pins for receiving control signals for controlling said semiconductor chip; and

second pins for inputting data to and outputting data from said semiconductor chip,

wherein all of said first pins are provided on a first side of said package and all of said second pins are provided on a second side of said package substantially perpendicular to said first side, said first pins and said second pins excluding pins for receiving power voltages.

14. A device comprising:

a board;

first signal lines provided on said board to extend straight in a first direction;

semiconductor packages connected to said first signal lines to share said first signal lines; and

second signal lines provided on said board to extend in a second direction substantially perpendicular to said first direction, said second signal lines being provided separately for each of said semiconductor packages,

wherein each of said semiconductor packages comprises:

first pins connected to said first signal lines; and

second pins connected to said second signal lines,

wherein all of said first pins are provided on a first side of each of said semiconductor packages and all of said second pins are provided on a second side of each of said semiconductor packages substantially perpendicular to said first side, said first pins and said second pins excluding pins for receiving power voltages.

18. A device comprising:

a first board;

first signal lines provided on said first board; and

a plurality of semiconductor devices mounted on said first board, each of said semiconductor devices comprising:

a second board;

second signal lines provided on said second board to extend straight in a first direction;

semiconductor packages connected to said second signal lines to share said second signal lines;

third signal lines provided on said second board to extend in a second direction substantially perpendicular to said first direction, said third signal lines being provided separately for each of said semiconductor packages; and

node portions provided at an end of said second signal lines and said third signal lines and arranged in a line on one side of said second board to be connected to said first signal lines,

wherein each of said semiconductor packages comprises:

first pins connected to said second signal lines; and

second pins connected to said third signal lines,

wherein all of said first pins are provided on a first side of each of said semiconductor packages and all of said second pins are provided on a second side of each of said semiconductor packages substantially perpendicular to said first side, said first pins and said second pins excluding pins for receiving power voltages.

In rejecting Appellants' claims, the Examiner relies on multiple references:

Murai	4,586,162	Apr. 29, 1986
Takeda et al. (Takeda)	5,319,591	Jun. 7, 1994
Werther	5,513,076	Apr. 30, 1996
Michael	5,572,457	Nov. 5, 1996

Claims 1-3, 6, 9 and 14-17 stand rejected under 35 U.S.C.

§ 103(a) as being obvious over Michael and Takeda. Claims 4, 5, 7, 8 and 10-13 stand rejected under 35 U.S.C. § 103(a) as being obvious over Michael, Takeda and Murai. Claim 18 stands rejected under 35 U.S.C. § 103(a) as being obvious over Michael and Werther. Rather than repeat the arguments of Appellants and the Examiner, we refer the reader to the Appellants' Briefs[1] and Examiner's Answer[2] for the respective details thereof.

OPINION

With full consideration being given the subject matter on appeal, the Examiner's rejection and the arguments of Appellants and the Examiner, for the reasons stated *infra*, we will reverse the Examiner's rejection of claims 1-18 under 35 U.S.C. § 103(a) as being unpatentable over combinations of Michael, Murai, Takeda and Werther.

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[1]Appellants filed an Appeal Brief on September 10, 1998. Appellants subsequently filed a Reply Brief on December 28, 1998.

[2]The Examiner, in response to Appellants' Brief, filed an Examiner's Answer on October 26, 1998.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) ("After a *prima facie* case of obviousness has been established, the burden of going forward shifts to the applicant"). If the Examiner fails to establish a *prima facie* case, the rejection is improper and accordingly merits reversal. ***Fine***, 827 F.2d at 1074, 5 USPQ2d at 1598.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments.

See ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444 ("In reviewing the Examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument"). Accordingly, we now consider the claims on appeal and focus first on the arguments related to claim 1.

In argument, Appellants assert that the prior art lacks the claim limitation that recites as follows:

> wherein all of said first pins [for receiving signals commonly used with said one or more semiconductor devices] are provided on a first side of said semiconductor device and all of said second pins [for being connected to signal lines which are not connected to said one or more semiconductor devices] are provided on a second side of said semiconductor device substantially perpendicular to said first side, said first pins and said second pins excluding pins for receiving power voltages.

Brief at pages 12-13. Appellants first assert that the Michael prior art does not teach, show or suggest the claim language that all of the first pins are provided on a first side and all of the second pins are provided on a second side of a semiconductor device. Brief at page 14. According to Appellants, Michael clearly teaches having both first and second pins on one side of the integrated circuit. Brief at

page 14. Next, Appellants argue that Takeda, similarly, does not show, teach, or suggest the claim limitation recited *supra*. Brief at page 15. Specifically, Appellants provide the example that the control pin WE of Takeda is not placed on a first side which is substantially perpendicular to the second side where pins Din, Dout are provided. Brief at page 15. Turning to the Murai prior art reference, Appellants contend that Murai also does not show, teach or suggest the claim limitation recited *supra*. Brief at page 21. Appellants state that Murai clearly teaches that the two sides of the memory device that are used are parallel to one another, and not perpendicular to one another. Brief at page 21. Finally, with respect to the Werther prior art, Appellants state that

> nothing in Werther shows, teaches or suggests that each semiconductor package comprises first pins connected to the second signal lines, second pins connected to the third signal lines or that all the first pins are provided on the first side of each semiconductor package and all the second pins are provided on the second side of each semiconductor package perpendicular to the first side.

Brief at page 25. In sum, Appellants assert that nothing in the combination of Michael, Takeda, Murai and Werther shows, teaches or suggests the perpendicular arrangement of the first

and second pins on first and second sides of a device or package as Appellants claim. Brief at page 25.

In response, the Examiner, acknowledging that Michael does not disclose first and second pins on two perpendicular sides of the device, looks to the Takeda prior art and asserts that Takeda's Figures 5 and 6 show the use of pins on all four sides of a memory device. Examiner's Answer at page 2. Because the use of pins on all four sides of a memory device is well known, the Examiner concludes that it would have been obvious to one of ordinary skill in the art to position different pins on different sides of a semiconductor device as taught by Takeda. Examiner's Answer, page 1.

Considering the Murai prior art, the Examiner references Murai's Figure 2, which illustrates a chip with data and address signal pins located on two different sides, and concludes that it would have been obvious to one of ordinary skill in the art to rearrange the location of pins on different sides of a semiconductor device. Examiner's Answer at page 3.

In examining the Werther prior art, the Examiner notes that it discloses the use of first and second boards and a

semiconductor package having pins on all four sides. Therefore, the Examiner concludes that it would have been obvious to arrange the signal lines and memory pins of Michael on two perpendicular sides of the board or to use more than one board.

An obviousness determination under 35 U.S.C. § 103 is based on underlying factual inquiries including the scope and content of the prior art, differences between the prior art and the claims at issue, and the level of ordinary skill in the art. ***Graham v. John Deere* Co.**, 383 U.S. 1, 13-14, 148 USPQ 459, 465 (1966). In addition, obviousness based on particular art references requires a showing of a suggestion or motivation to combine the teachings of those references, although it need not be expressly stated. ***Riverwood Int'l Corp. v. Mead Corp.***, 212 F.3d 1365, 1366, 54 USPQ2d 1763, 1765 (Fed. Cir.), cert. denied, 531 U.S. 1012 (2000).

In determining the scope of independent claim 1, we first note that the claim contains at least three limitations: 1) first pins for receiving signals common to one or more

semiconductor devices; 2) second pins connected to signal lines and not connected to one or more semiconductor devices; and 3) wherein the first pins are provided on a first side, the second pins are provided on a second side and the second side is substantially perpendicular to the first side.

Our review of the Michael prior art discloses that Michael's Figure 2 illustrates control signal pins, e.g., RAS, CAS, WRITE and data-input/output pins, e.g., DI, DO. However, we do not find that the control and data pins of Michael are respectively provided on sides that are "substantially" perpendicular to each other.

Turning to the Takeda prior art, we note that Takeda also discloses control pins, e.g. WE, RAS, CAS, and data-input/output pins, e.g. DIN, DOUT. However, as in Michael, we find that the control and data pins of Takeda are not provided on sides that are “substantially” perpendicular to each other. In particular, Takeda's Figure 6 illustrates a configuration that shows the WE control pin and the DIN, DOUT data-input/output pins on the same side.

Considering the Murai prior art, Murai’s Figure 2 illustrates control (address) pins on one side and data pins

on another side. However, we do not find that any of Murai's Figure 2 configurations disclose a pin arrangement wherein the control pins and data pins are respectively arranged on perpendicular sides.

Werther discloses the use of first and second boards. However, we also do not find any teaching or suggestion in Werther of a pin arrangement wherein the control and data pins are arranged on perpendicular sides.

It is the burden of the Examiner to establish why one of ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art. **In re Sernaker**, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). The Examiner has failed to persuasively show and we find no evidence of any teaching or suggestion in Michael, Takeda, Murai or Werther of Appellants' claim 1 limitations. We further find no implicit or explicit suggestion or reason to combine any of these prior art references in an obviousness determination. We conclude therefore that the Examiner has failed to establish a ***prima facie*** case of unpatentability with respect to claim 1. Claims

2-9 depend from claim 1. Accordingly, we reverse the Examiner's rejection of claims 1-9.

Turning now to consider the scope of independent claim 10, we note that it comprises limitations similar to claim 1: first pins for receiving control signals, second pins for inputting and outputting data and wherein the first pins are provided on one side, the second pins are provided on a second side and the sides are substantially perpendicular to each other.

We have already established that neither Michael, Takeda, nor Murai teaches or suggests, either individually or in combination, first and second pins arranged on perpendicular sides. Therefore, based on this prior reasoning, we reverse the Examiner's rejection of claims 10-13, as obvious over the combination of Michael, Takeda, and Murai.

Turning now to independent claim 14, it also comprises similar limitations common to independent claims 1 and 10. Specifically, claim 14 recites first pins and second pins, wherein first pins are provided on a first side of a semiconductor and second pins are provided on a second side

and the first and second sides are substantially perpendicular to each other.

We have already established that neither Michael, Takeda, Murai nor Werther teaches or suggests, either individually or in combination, first and second pins arranged on perpendicular sides. Therefore, based on this prior reasoning, we reverse the Examiner's rejection of claims 14-17 as obvious over the combination of Michael, and Takeda.

Considering independent claim 18, it likewise includes the claim limitation common to independent claims 1, 10, and 14. Specifically, claim 18 recites first pins and second pins, wherein first pins are provided on a first side of a semiconductor and second pins are provided on a second side and the first and second sides are substantially perpendicular to each other.

Having already established that neither Michael nor Werther teaches or suggests, either individually or in combination, first and second pins arranged on perpendicular sides, we reverse the Examiner's rejection of claim 18 as obvious over the combination of Michael and Werther.

In summary, based on the foregoing, we reverse the Examiner's rejection of claims 1-18 as unpatentable over combinations of Michael, Takeda, Murai and Werther under 35 U.S.C. § 103.

REVERSED

JERRY SMITH Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES

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